A 2–20 GHz High-Gain Monolithic HEMT Distributed Amplifier

STEVE G. BANDY, CLIFFORD K. NISHIMOTO, CINDY YUEN, ROSS A. LARUE, MARY DAY, JIM ECKSTEIN, ZOILO C. H. TAN, CHRISTOPHER WEBB, AND GEORGE A. ZDASIUK, MEMBER, IEEE

Abstract —A low-noise 2–21 GHz monolithic distributed amplifier utilizing 0.35-micrometer-gate-length HEMT devices has achieved 12±0.5 dB of gain. This represents the highest gain reported for a distributed amplifier using single FET gain cells. A record low noise figure of 3 dB was achieved midband (4–12 GHz). The circuit design utilizes five HEMT transistors of varying width with gates fabricated by E-beam lithography. The same amplifier fabricated with 0.35-μm-gate-length MESFET's in place of the HEMT devices resulted in 9.5±0.5 dB of gain across the 2–20 GHz band. This record performance level for a MESFET distributed amplifier is used to determine that the use of HEMT devices rather than the small gate lengths is primarily responsible for the HEMT amplifier performance.

I. Introduction

This paper is the first to report results of a working monolithic distributed amplifier utilizing 0.35-μm-gate-length HEMT's. A number of authors have previously reported reactively tuned, narrow-band amplifiers using discrete high electron mobility transistors (HEMT's) [1], [2]. Also, many workers have reported monolithic distributed amplifiers utilizing 0.50-μm-gate-length MESFET's that have achieved 7–8 dB gain and a noise figure of approximately 5 dB in the 2–20 GHz band [3]. By replacing the conventional MESFET with high-performance, 0.35-μm-gate-length HEMT's, significant improvements in gain and noise figure are achievable. Fig. 1 shows the HEMT device structure used in this work. The AlGaAs epitaxial layer is doped higher ($\sim 2\times10^{18}/cm^3$) than the active layer in a MESFET; hence HEMT's usually possess higher intrinsic transconductance (g_m), as high as 500 mS/mm but with a concomitant higher gate capacitance (C_{gs}). Additionally, the gate-to-drain breakdown voltage for the HEMT may be reduced because of the higher doping, impacting the power performance.

II. Circuit Design

Fig. 2 shows the equivalent circuit model for discrete 0.3-×150-μm-gate-length HEMT's fabricated in our lab. The model is for maximum gain bias conditions. The devices were first characterized by s-parameter measurements in the common-gate, common-source, and common-drain configurations from 2 to 18 GHz. A single equivalent circuit model is then constrained to fit the three sets of data. Details of the procedure are described elsewhere [4], but it should be noted that this particular device had a g_m of 520 mS/mm. Because the doping is high, C_{gs} would normally be high, but is kept to a minimum by reducing the gate length.

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The authors are with the Device Laboratory, Varian Research Center, Palo Alto, CA 94303.

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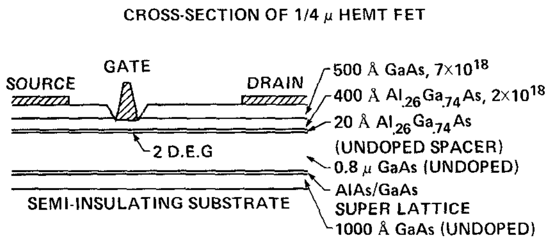

Fig. 1. Cross section of high electron mobility transistor fabricated in the lab. A noise figure of 1.35 dB and an associated gain of 12 dB were measured at 18 GHz.

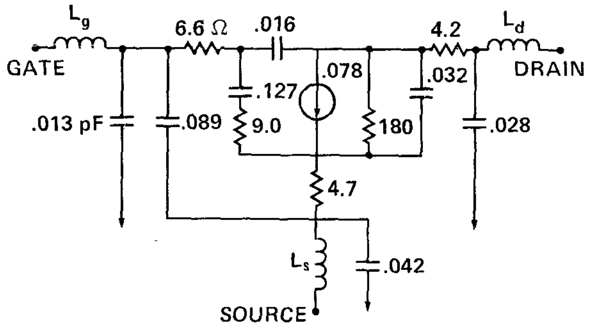

Fig 2. Equivalent circuit model of HEMT device biased for maximum gain. The intrinsic transconductance is 520 mS/mm.

The same procedure was used to obtain the device model for the same HEMT biased for minimum noise, resulting in an intrinsic g_m of 56 mS (373 mS/mm), a C_{gs} of 0.085 pF, and an r_{ds} of 238 Ω. The remaining parameters were close to the Fig. 2 values.

Both the high-gain and low-noise models were used in the design of five HEMT distributed amplifiers in the 2–20 GHz band. Maximum gain, gain flatness, and minimum return loss were traded off against each other in the amplifier design optimizations. Finally, two amplifier designs for each model were obtained, one for maximum gain and one for maximum return loss.

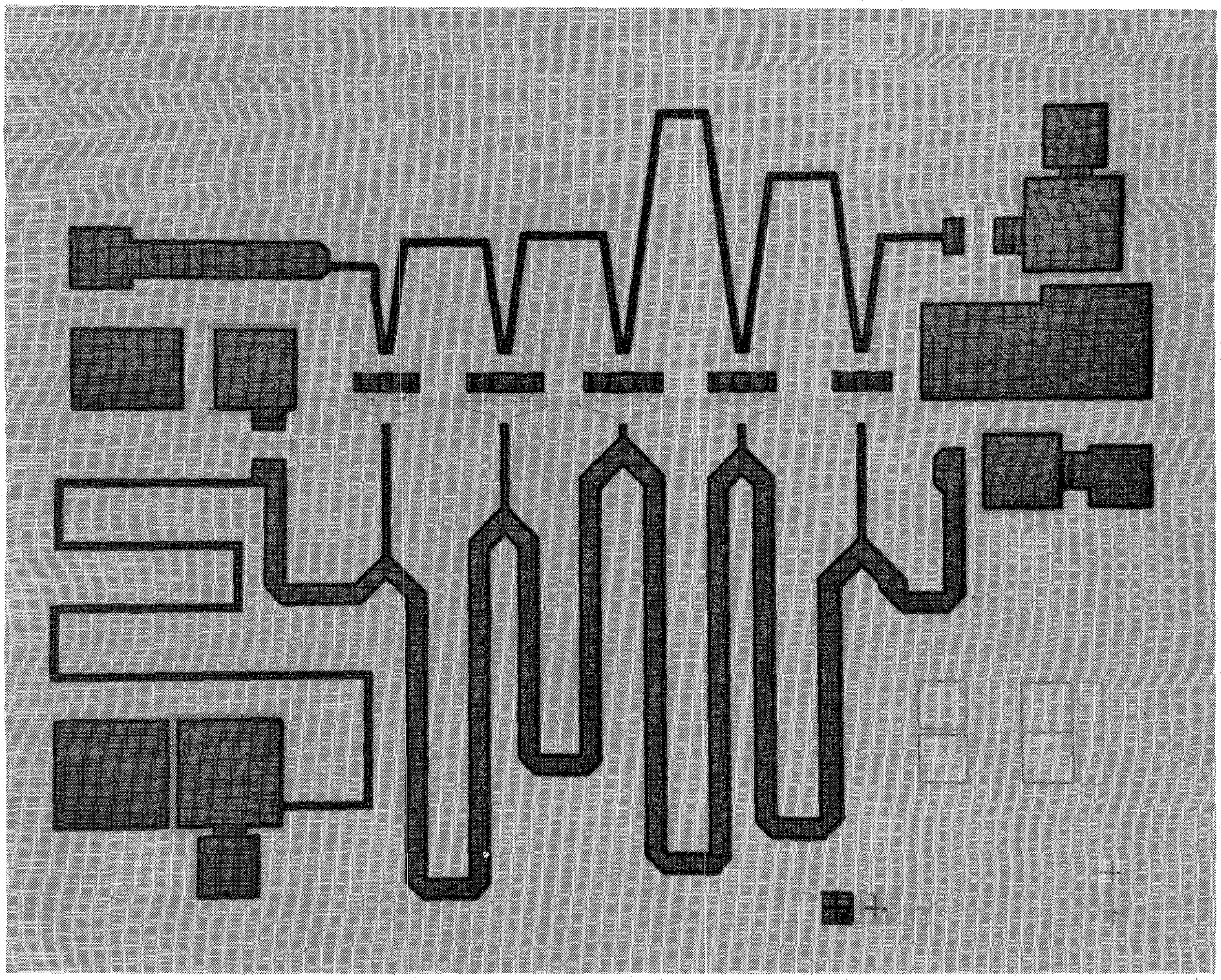

Fig. 3. Photomicrograph of HEMT amplifier. Chip size: 2.3×1.7 mm.

CAD was used to optimize 24 circuit design parameters including five HEMT gate widths and 12 gate and drain line lengths. By allowing the HEMT's to vary in width and the gate and drain line sections to vary in length, the gain is enhanced by 1–2 dB and an improved return loss is achieved when compared to the conventional constant-K design. Additional details of this variable device width design approach are found elsewhere [4], but generally the wider HEMT's are located in the center of the amplifier.

Using π-gate-configured FET's, the total device periphery is 620 μm for the amplifier using the maximum gain bias model and 698 μm for the amplifier using the minimum noise bias model. A photomicrograph of the complete chip for the amplifier based on the maximum gain bias model is shown in Fig. 3. The transmission line widths are 12.7 μm for the gate line and 45.2 μm for the drain line. To be noted are the variable lengths of the gate and drain line sections. The longest section in the gate line is 1117 μm (35.4° at 10 GHz) and the longest section in the drain line is 1914 μm (60.6° at 10 GHz). The MMIC has on-chip gate and drain line terminations and biasing networks.

If the gate and drain line losses per unit length were zero or equal, filter theory would suggest equal-width devices except for tapering on the ends to maximize return loss, as shown in Fig. 4(a). Fig. 4(b) shows a simple gain expression for a two-FET amplifier which is optimized for relative device widths and generalized to successive device pairs in a multiple-FET distributed amplifier. If W_n and W_{n+1} are the successive device widths of the nth and $(n+1)$th FET's and if r_{gl} and r_{dl} are the gate and drain line shunt resistances per unit length, then

$$\frac{W_n}{W_{n+1}} \cong \frac{r_{dl}}{r_{gl}} \tag{1}$$

for optimum gain. R_0 is the transmission line characteristic impedance, and g_{ml} the transconductance per unit width W. The MESFET distributed amplifiers fabricated in our labs ($L_g \leqslant 0.6$ μm) have been dominated by drain-line loss ($r_{dl} < r_{gl}$), and have had the ideal profile shown in Fig. 4(a) skewed towards increasing device widths so that the last width is nearly equal to the middle device widths, as shown in Fig. 4(b) and predicted by (1). On the other hand, the superior output conductance of the HEMT device (as will be discussed in Section IV) enables the ratio in (1) to be nearly unity at the upper band edge, thereby returning the width distribution back to the ideal profile of Fig. 4(a). This is indeed the case, as shown for the opti-

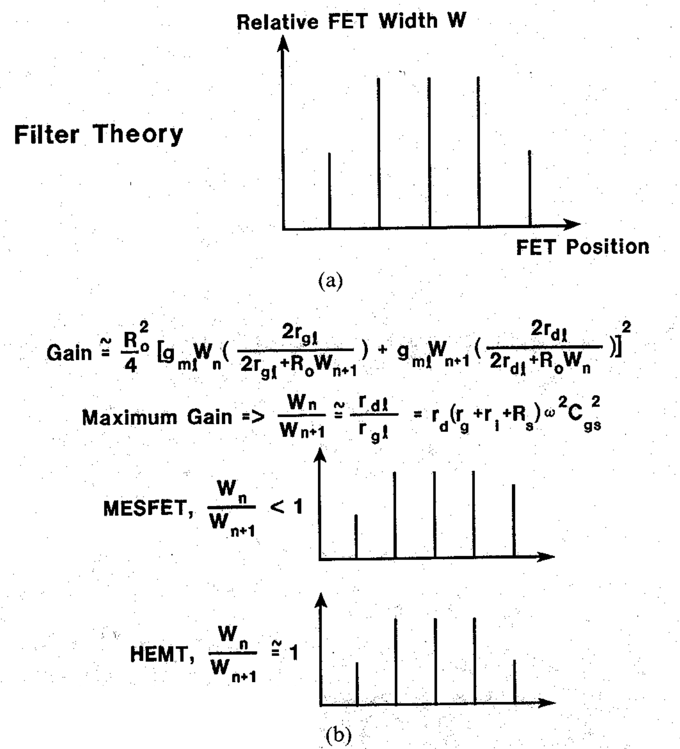

Fig. 4. Variable-width amplifier design by (a) filter theory and with (b) transmission line loss.

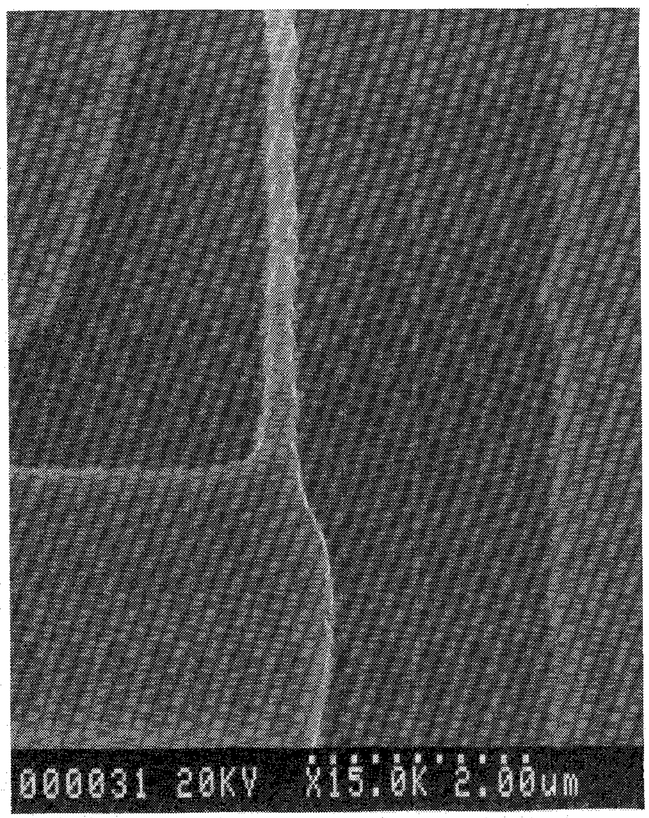

Fig. 5. Photomicrograph of gate and gate lead of a typical submicrometer HEMT device.

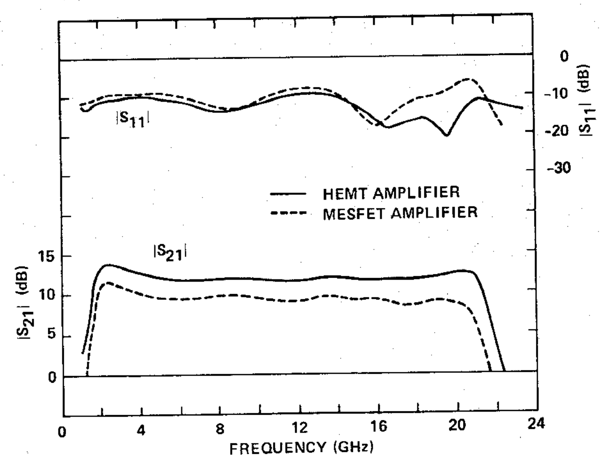

Fig. 6. Gain and return loss of working HEMT and MESFET amplifiers biased for maximum gain.

mized design of Fig. 3, and verifies the superior output conductance of HEMT's over that for MESFET's.

III. Fabrication

The HEMT layers shown in Fig. 1 were grown by MBE at 565°C. The GaAs is unintentionally doped n-type at about $1\times10^{14}/\text{cm}^3$. A five-period AlAs/GaAs superlattice is grown midway into the buffer layer in an attempt to reduce dislocations and improve surface morphology.

Standard processing techniques were used for most of the HEMT distributed amplifier fabrication. Isolation was achieved with a 2500-Å mesa etch. Fig. 5 shows a photomicrograph of a typical submicron gate fabricated in the lab using E-beam lithography. Gate exposures in PMMA were achieved with a commercial E-beam exposure system, after which a shallow gate recess etch to the first layer of AlGaAs was performed. In order to achieve good grounding of the source, 50×50-μm backside vias were fabricated using reactive ion etching. All other process steps used conventional metallization, liftoff, and pulse plating techniques.

IV. Measured Gain Performance

As shown in Fig. 3, the layout of the circuit is compatible with RF wafer probing techniques. Fig. 6 shows the gain and return loss obtained for the amplifier design using the maximum gain bias model, using the Cascade Microtech RF wafer prober. 12 ± 0.5 dB of gain over the 2–21-GHz bandwidth was achieved. The drain and gate bias were adjusted for maximum gain ($V_d=3.5$ V, $V_g=-0.15$ V, $I_{ds}=106$ mA). The gain, bandwidth, and return loss agree well with the simulated result, indicating that capacitive and inductive coupling between the lines, which was not modeled, is not significant (a run with deep RIE-etched grooves between the lines showed no discernible difference in performance).

Another design version using the same maximum gain bias model gave a better return loss of -14 to -15 dB for the same 12 dB of gain, but the gain experienced a sudden step drop to 10.5 dB at 18 GHz. When biased for maximum gain, the design version using the low-noise bias model showed only ~0.5 dB less gain than shown in Fig. 6, with the return loss being essentially the same.

The HEMT device is particularly suited for achieving high gain in distributed amplifiers because of its higher transconductance and lower output conductance (per unit g_m) compared with the MESFET. The higher transconductance is a result of the increased saturated velocity of the two-dimensional electron gas (2DEG) layer [5], [6] and the fact that AlGaAs can be doped higher than GaAs without compromising the gate breakdown voltage (due to the larger bandgap). The lower output conductance is a result of the two-dimensional nature of the conduction electrons.

The high transconductance means smaller device widths, which translates to smaller MMIC chip sizes, especially for mm-wave applications.

The distributed amplifier gain is usually 1–2 dB below the maximum available gain (MAG) at the upper band-edge frequency. At this frequency, the power to the gate line termination falls to nearly zero, and the power to the drain line termination is mostly reflected due to the mismatch caused by the increasing drain line impedance as the line cutoff frequency is approached.

Ignoring feedback, MAG is given by

$$\text{MAG} \cong \frac{g_m^2}{4\omega^2 C_{gs}^2 r_i g_{ds}} \qquad (2)$$

so one would expect the amplifier gain to be 1 or 2 dB below this expression when evaluated at the upper band edge. In this expression, r_i is the input series resistance and g_{ds} is the output conductance. The amplifier gain, then, is roughly proportional to

$$G \propto \left(\frac{g_m}{C_{gs}}\right)^2 (g_m r_{ds}) \qquad (3)$$

assuming $r_i \propto g_m^{-1}$. Fig. 7 shows the $g_m r_{ds}$ factor comparison between 0.35-μm-gate-length HEMT's and MESFET's fabricated in our lab when biased at zero gate bias. HEMT's appear to enjoy an advantage of about 1.5 for this factor. It also appears that r_{ds} for HEMT devices is inversely proportional to g_m. Even though r_{ds} is quite low in Fig. 2, the $g_m r_{ds}$ product is still superior to that for MESFET's. Because the epitaxial layer thickness a is so much smaller for HEMT devices, the larger L_g/a ratios result in higher values of r_{ds} [8, fig. 13].

If the gate side wall capacitance is accounted for in the manner of [13], the other factor in (3) is given by

$$\frac{g_m}{C_{gs}} \cong \frac{v_s}{L_g + \pi a} \qquad (4)$$

where a is the epitaxial thickness under the gate. For $L_g = 0.35$ μm and $a = 600$ Å for MESFET's and 300 Å for HEMT's, for example, (4) gives a factor of 1.2 improvement for HEMT's for the same saturated velocity. This factor, along with the $g_m r_{ds}$ factor, gives a 3.4-dB improvement in gain for HEMT's by (3). The superior performance of the HEMT may thus be due more to these factors than to an increased saturated velocity, and it may be that a pulse-doped MESFET may perform nearly as well.

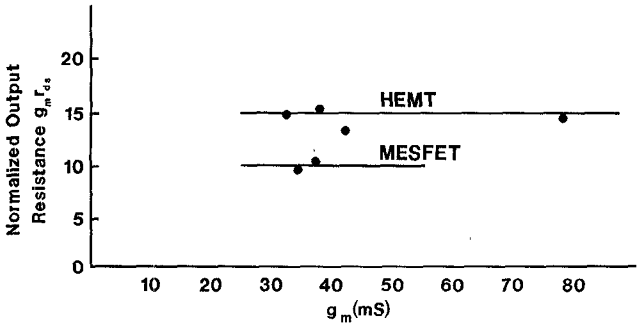

Fig. 7. Output resistance comparison between HEMT's and MESFET's ($L_g \cong 0.35$ μm).

While it is true that the small 0.35-μm gate lengths are partially responsible for the improved performance of Fig. 6, simulations show that due to the increase of g_{ds} with decreasing gate length, only marginal gain improvement using such small gate lengths is possible with MESFET's (see Section VI). This necessitates going to a scheme such as the cascode configuration [4] to circumvent this problem. The lower output conductance of the HEMT device enables the advantages of a shorter gate length to be realized in the distributed amplifier configuration without resorting to a more complicated and potentially unstable gain cell. Simulations using the HEMT device in the cascode configuration indicate that gains of 15 dB over the 2–20 GHz bandwidth can be achieved.

V. Amplifier Noise Performance

This section will discuss HEMT low-noise performance, HEMT suitability for broad-band low-noise applications, and the measured noise performance of the distributed amplifier.

The narrow-band noise performance of discrete HEMT devices fabricated in our facility is typically a minimum noise figure of 1.25–1.5 dB at 18 GHz, with an associated gain of 11–12 dB for gate lengths in the 0.3–0.35 μm range.

The noise figure of a FET device can be expressed by [8]

$$F = 1 + \frac{r_n}{R_s} + \frac{g_n}{R_s}\left[\left(R_s + \sqrt{R_{s,\text{opt}}^2 - \frac{r_n}{g_n}}\right)^2 + \left(X_s - X_{s,\text{opt}}\right)^2\right]$$

where r_n and g_n are the noise resistance and conductance, respectively, $Z_s = R_s + jX_s$ is the source impedance, and $R_{s,\text{opt}} + jX_{s,\text{opt}}$ is the optimum source impedance for minimum noise. The equation shows that, under conditions of noise mismatch such as encountered in a distributed amplifier, the largest noise bandwidths occur when g_n and the ratio $X_{s,\text{opt}}/R_{s,\text{opt}}$ are the smallest. Empirical data have been taken [9] which demonstrate that HEMT devices have lower values of both g_n and the ratio $X_{s,\text{opt}}/R_{s,\text{opt}}$ than MESFET's. Accordingly, HEMT devices should be better suited for broad-band low-noise applications.

Fig. 8 compares the gate bias dependence of the minimum noise figure and associated gain at 12.4 GHz for both the HEMT and MESFET devices in a 50-Ω system

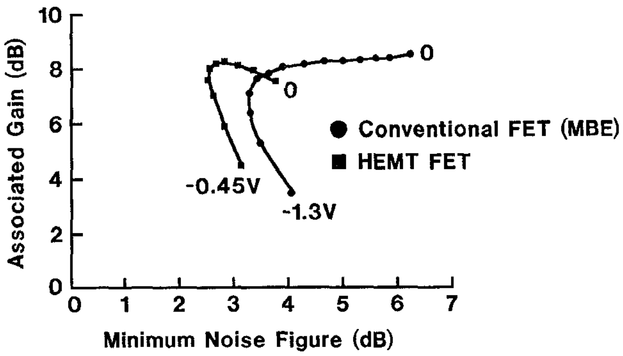

Fig. 8. 12-GHz FET performance in a 50-Ω system with varying gate bias.

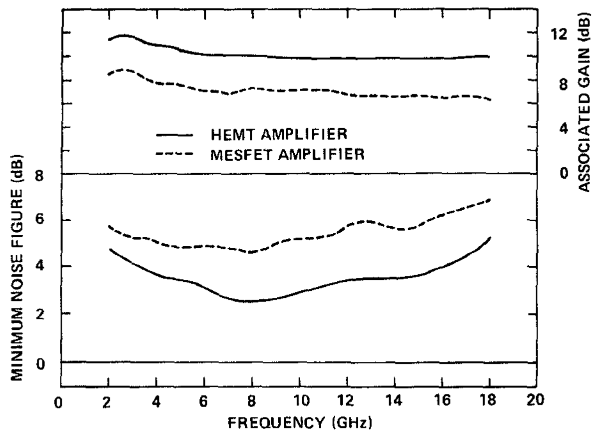

Fig. 9. Noise performance and associated gain of the HEMT and MESFET amplifiers.

(no input or output matching), which gives some indication of what would be experienced in the environment of a distributed amplifier. Both devices have a 0.4-μm gate length and the HEMT has a 50-Å AlGaAs spacer layer. The HEMT has an advantage of approximately 1 dB in both the minimum noise figure and the associated gain under these conditions.

Fig. 9 shows the minimum noise performance for the amplifier. The low value of approximately 3 dB over the 4–12 GHz midband region exceeds previously reported performance for distributed amplifiers by several dB for the same bandwidth [3], [10], [11]. The associated gain of around 10 dB is only 2 dB below the maximum gain. Fig. 9 shows the usual noise skirts due to the gate termination resistor on the low-frequency end and the transmission line cutoff frequency on the high end of the band.

The maximum gain bias noise performance is only slightly higher, being 0.2 dB and 0.5 dB higher at the low and high ends of the band, respectively.

The amplifier was designed for maximum gain rather than minimum noise figure for purposes of achieving a multistage gain of 20 dB with as few stages as possible. The minimum noise figure for the amplifier using the minimum noise bias model was measured to be ~ 0.5 dB higher than that for the amplifier using the maximum gain bias model. This result emphasizes the need for an accurate noise parameter model for the HEMT device in order to achieve optimum low-noise performance. Optimization using the considerations in [12] in conjunction with a suitable computer simulation program for noise sources should give a design which further reduces the noise figure.

VI. MESFET Amplifier Performance

To ascertain what part of the gain improvement of the HEMT amplifier over previously published results [3], [10], [11] is due to the use of 0.35-μm gate lengths and what part is due to the use of HEMT devices, an amplifier run was made with MESFET devices (MBE growth with $5\times 10^{17}/\text{cm}^3$ active layer doping) having 0.35-μm gate lengths.

An optimized CAD simulation for a distributed amplifier using the device model for the 0.35-μm-gate-length MESFET results in 9.5-dB gain from 2 to 20 GHz. Fig. 6 shows the measured gain response for the MESFET version of the amplifier using the same HEMT amplifier mask set. This 9.5 ± 0.5-dB measured performance is the highest reported for a MESFET amplifier, and is, of course, primarily the result of the 0.35-μm gate lengths employed. The fact that this gain is virtually the same as that obtained for the optimized CAD simulation indicates that very little improvement would be achieved with a MESFET optimized layout. The 9.5-dB response indicates an improvement of only 1.5 dB over the 8-dB gain obtained for the distributed amplifier employing 0.5-μm-gate-length FET's previously fabricated in our lab, and far short of the 12-dB performance of the HEMT version.

Even more notable is the difference in noise performance between the use of MESFET's and HEMT's in distributed amplifier applications. Fig. 9 shows a difference of ~ 2 dB lower noise figure for the HEMT amplifier version. As discussed previously, since the HEMT version was not optimized for noise, it is probably safe to say that this large difference would probably not be significantly reduced by a design optimized for MESFET gain in the same way that the Fig. 3 design was optimized for HEMT gain.

Also shown in Fig. 9 is that the associated gain for the MESFET amplifier was measured to be 7 dB, which is 3 dB lower than the associated gain for the HEMT amplifier.

It seems clear, then, that the bulk of the performance improvement measured for the HEMT distributed amplifier is due to the use of HEMT devices in place of MESFET devices.

VII. Measured Output Power Performance

The 1-dB compression power and the third-order intermodulation intercept point were measured for the HEMT and MESFET amplifiers at 10 GHz, as shown in Fig. 10. When biased at maximum gain, the 1-dB compression power for the HEMT amplifier was measured to be 17 dBm at 10 GHz. The third-order intermodulation intercept point was measured to be 27 dBm under the same conditions. The 10-dB difference between these two measurements is close to the theoretical difference of 10.6 dB [7].

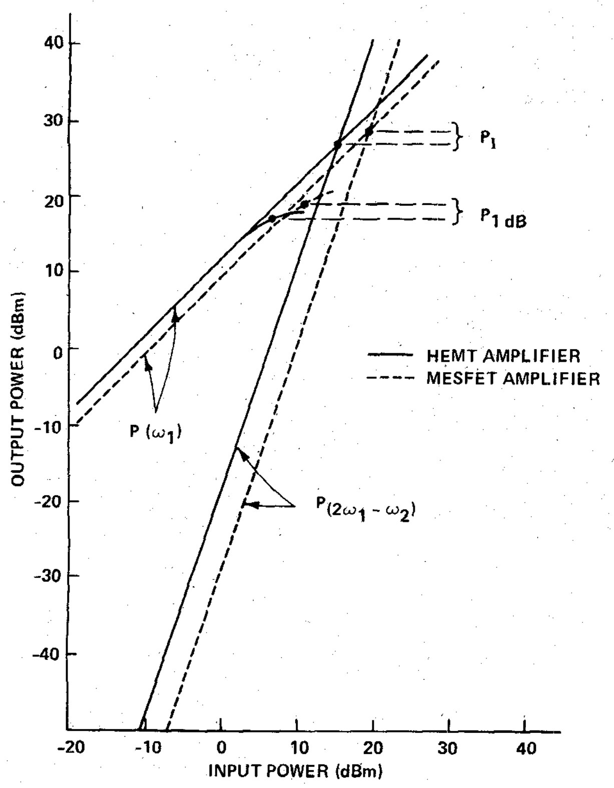

Fig. 10. Output power performance comparison of HEMT and MESFET amplifiers.

Fig. 10 shows that for close to the same bias current and voltage, MESFET distributed amplifiers have around 2 dB higher compressed power and third-order intercept levels when biased for maximum gain. Presumably, the lower values for the HEMT version are due to a much higher nonlinearity in the g_m versus gate bias characteristic. Occasionally, the HEMT amplifier power levels fall even further (sometimes by 5 dB) below those of the MESFET amplifier, perhaps because of increased gate recess etch nonuniformity over the width of a single device. HEMT devices, because of their much higher doping and resulting thinner layers, show an increased sensitivity to etch depth variations over the FET width than do MESFET's.

VIII. Conclusions

The results presented in this paper indicate that by using high-performance, low-noise HEMT's with gates defined by E-beam lithography, record improvements in gain and noise figure can be achieved for broad-band distributed amplifiers. A gain of 12 dB $\pm$0.5 dB from 2 to 21 GHz and a midband noise figure of 3 dB have been achieved on a working HEMT amplifier. This represents the highest gain and lowest noise figure reported for a distributed amplifier using single FET's for the gain cell.

The use of MESFETs with E-beam-defined gates in the same amplifier configuration resulted in 9.5$\pm$0.5 dB of gain across the 2–20 GHz band. This represents a record performance level for a MESFET distributed amplifier. Comparison with the HEMT amplifier performance indicates that the bulk of the performance improvement measured for the HEMT amplifier over previously published MESFET performance levels is due to the use of HEMT devices in place of MESFET devices rather than the use of 0.35-μm gate lengths. The HEMT device is able to outperform its MESFET counterpart with the same gate length in distributed amplifier applications by virtue of its higher transconductance and lower output conductance.

Acknowledgment

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Steve G. Bandy received the B.S. degree in electrical engineering from Walla Walla College in 1965 and the Ph.D. degree in electrical engineering from Stanford University in 1970.

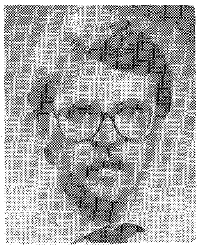
He joined the Varian Research Center of Varian Associates in Palo Alto, CA, in 1969 and has since been responsible for advanced studies on III–V discrete FET's for use in low-noise and power applications. In 1975, he was appointed manager of the Microwave Device Group, and in 1985 he was appointed manager of the Microwave Circuits and Devices Group of the Research Center.

Dr. Bandy is a member of Sigma Xi.

Clifford K. Nishimoto is a process engineer at Varian Associates Research Center, Palo Alto, CA. He received the B.S. degree in electronic engineering from California Polytechnic State University at San Luis Obispo in 1973. He has been involved with the fabrication and testing of GaAs MESFET's, AlGaA/GaAs MODFET's, and HEMT MMIC's for microwave applications. His work has also included electron-beam lithography.

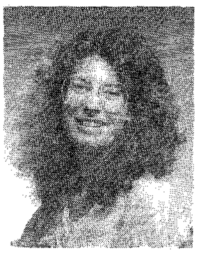
Cindy Yuen received the B.S. degree in physics in 1972 from Tsing Hua University in Taiwan and the M.S. and Ph.D. degrees in physics from Stanford University in 1974 and 1978, respectively.

From 1978 to 1982 she worked in the Radiation Division of Varian Associates, Inc., where she has been involved in the designs of the electron linear accelerator and the microwave hyperthermia system. In 1982 she joined the Varian Associates Central Research Laboratories, where she is currently engaged in the development of GaAs monolithic microwave integrated circuits.



Ross A. LaRue received the B.S. degree in physics/mathematics at San Jose State University in 1977 and the M.S. degree in physics from the University of Illinois in 1979. He is currently an honors co-op student at Stanford University in the Applied Physics Department.

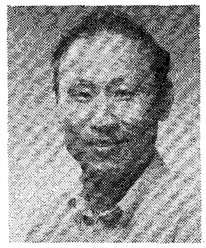
He joined Varian Associates in 1979 and worked for three years on novel high-efficiency III–V photovoltaic devices. In 1983, he began work in the microwave field and published an article on a distributed FET model. He is currently working on an HEMT version of the cascode distributed amplifier.



Mary Day has been involved in the development of state-of-the-art GaAs monolithic microwave integrated circuits since 1980. Her expertise is in developing high-resolution photolithography processes and in thin-film deposition technologies. For this work Ms. Day takes credit for developing the on-chip capacitors, resistors, and the via hole technology.

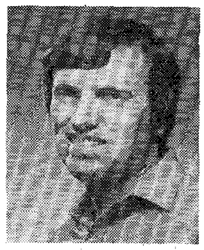
Jim Eckstein is Manager of the Molecular Beam Epitaxy group at Varian Research Center. He received the B.A. degree in physics from St. Olaf College in 1973 and the Ph.D. degree, also in physics, from Stanford University in 1978, where he studied spectroscopic techniques using picosecond laser sources.

After working for several years as a research associate in the Free Electron Laser group at Stanford, he joined Varian Associates, where he has been involved in device and materials related research. His current interests include III–V materials growth, including heterostructure studies and novel techniques in epitaxy, as well as the growth of thin-film superconducting layers using MBE techniques.



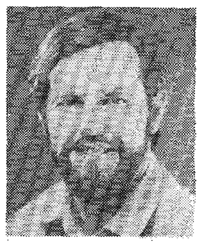
Zoilo C. H. Tan received the B.S. degree in chemical engineering from Cheng Kung University, Taiwan, in 1963; the M.S. degree in physical chemistry from the University of Arkansas in 1966, and the Ph.D. degree in nuclear chemistry from the Massachusetts Institute of Technology in 1969.

His research interests are in the development of resist and processes for advanced microlithography. He was the key inventor of Kodak MX 771 X-ray resist and ZX 784 e-beam resist. Following a brief career as staff scientist at Synertek Inc., he joined the Gate Array Division of Fairchild Semiconductor in 1985, where he was engaged in various resist processes for both optical and e-beam lithography. He is currently Manager of the E-Beam Center, Varian Research Center, Varian Associates, Inc., Palo Alto, CA.



Christopher Webb studied at Cambridge University, obtaining the M.A. Honors degree in natural sciences (physics). Subsequently he received the Ph.D. degree in surface studies from Imperial College, London.

After further work in the field of surface science both in England and the U.S., he joined the MBE group at Varian Research Center in 1984 to carry out research on GaAs based semiconductors. Here he has been involved in the development of device quality materials, as well as more basic studies, including surface defects, superlattices and RHEED oscillations. Most recently he has participated in a project to grow thin-film high-T_c superconductors. He has published more than 20 scientific papers.



George A. Zdasiuk (S'80–A'80–M'81) received the B.Sc. degree in engineering science and the M.Sc. degree in physics from the University of Toronto in 1974 and 1975, respectively. He subsequently received the Ph.D. degree in applied physics from Stanford University in 1981. His thesis research was in the area of quantum electronics.

In 1980, he joined Varian Associates' Solid State Laboratory. He has been involved in the development of submicron GaAs FET devices, microwave characterization techniques, and the design and fabrication of GaAs monolithic microwave integrated circuits. Currently, he is the Associate Director of the Device Laboratory at Varian Research Center.

Dr. Zdasiuk is a member of the Institute of Electrical and Electronics Engineers and the American Physical Society.